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EXAMINER	
MONDT, JOHANNES P	

ART UNIT	PAPER NUMBER
3663	

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10/29/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/753,524	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Johannes P. Mondt	3663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-23,25 and 42-70* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-23, 25 and 42-70* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/2/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Amendment filed 8/20/07 forms the basis for this Office Action. In said Amendment applicant substantially amended claims 21-23, 23 and 42-64 through substantial amendment of independent claims 21, 47 and 56; and added new claims 65-70.

Comments on Remarks are included below under "Response to Arguments".

Information Disclosure Statement

The examiner has considered all items listed in the Information Disclosure Statement filed 7/2/2007. A signed copy of Form PTO-1449 is herewith enclosed.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. ***Claims 21-23, 25 and 42-70*** rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

2. Specifically, the "first lattice image" and "second lattice image" as recited in independent claims 21, 47 and 56, are indefinite concepts within the context of the invention as disclosed, because "image" relies on a particular correspondence with the actual, i.e., true, source of the image, while said correspondence has not been adequately disclosed. In particular, the resolution at which the image is made falls short of a definite disclosure because the term "high" in "high resolution TEM" is not defined

by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. Nor has Applicant provided any quantitative measure by which the image from HRTEM of his invention distinguishes from the prior art: the occurrence of spaces identified by the Specification as due to dangling bonds, between the crystal grain edges of otherwise abutting crystal grains appears, in light of the Specification, to be what the invention avoids, but in what measure is entirely unclear and is left entirely unspecified. The occurrence of dangling bonds per unit surface area of the grain boundaries in the polycrystal in the invention has not been quantified other than the discussion of Figures 17A-B pertaining to the invention juxtaposed with Figures 17C-D characterizing the prior art. Yet the resolution at which a specific quantitative statement on the number of dangling bonds per surface area of grain boundary is made to distinguish the invention from the prior art is critical for any definiteness of the claim language. Yet the Specification does not provide any quantitative measure in this regard. For instance, Applicant merely states that in the prior art there are "many traps" (par. [0068]) while in the invention "lattice defects such as unpaired (dangling) bond are not formed ([0066]). This characterization of the crucial distinction between the invention and the prior art falls far short of being definite.

3. The term "high" in "high resolution TEM" in ***claims 65-67*** is a relative term which renders the claim indefinite. The term "high" in "high resolution TEM" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite

degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. Nor has Applicant provided any quantitative measure by which the image from HRTEM of his invention distinguishes from the prior art: the occurrence of spaces identified by the Specification as due to dangling bonds, between the crystal grain edges of otherwise abutting crystal grains appears, in light of the Specification, to be what the invention avoids, but in what measure is entirely unclear and is left entirely unspecified. The occurrence of dangling bonds per unit surface area of the grain boundaries in the polycrystal in the invention has not been quantified other than the discussion of Figures 17A-B pertaining to the invention juxtaposed with Figures 17C-D characterizing the prior art. Yet the resolution at which a specific quantitative statement on the number of dangling bonds per surface area of grain boundary is made to distinguish the invention from the prior art is critical for any definiteness of the claim language. Yet the Specification does not provide any quantitative measure in this regard. For instance, Applicant merely states that in the prior art there are "many traps" (par. [0068]) while in the invention "lattice defects such as unpaired (dangling) bond are not formed ([0066]). This characterization of the crucial distinction between the invention and the prior art falls far short of being definite.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

1. ***Claim 21, 42- 43, 47 and 51-52*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki (JP 08-288515 A) (previously cited, with family member Iwasaki (USPAT 5,759,879) serving again as translation) in view of either Gates et al (5,830,538).

Iwasaki teaches (whole document, especially title, abstract, "Field of the Invention", column 1, lines 7-20, and Examples 1-2, columns 7-12; Figures 2-3) a semiconductor film 22 (column 10, lines 45-48) over a substrate 16 (loc.cit.) and comprising a source region and drain region (both 26N; see column 10, line 50) and a channel formation region 26i (column 10, lines 49-50) provided between said source and drain regions; and a gate electrode 25 (column 10, line 55) provided adjacent to said channel formation region with a gate insulating film 24 (column 10, line 54) therebetween; wherein lattices are continuously connected to each other at a grain boundary 23 (Figure 3F and column 12, lines 17-18) of said semiconductor film, inherently so, because a grain boundary is a boundary, i.e., a line, point or plane that indicates or fixes a limit or extent, between two grains, i.e., crystal grains; said crystal grains inherently

having spatial extent, as otherwise their defining property, i.e., spatial periodicity, could not possibly exist; the lines denoting the grain boundaries in Figure 3F thus denote the limits on either side of the crystal grains connected by their common grain boundaries, implying continuity across said grain boundaries; hence the lattices of said grains, extending by definition of the grains over their entire spatial domain, are continuously connected to each other at the grain boundaries of said semiconductor film.

Although Iwasaki does not explicitly teach the limitation that said semiconductor film comprises first and second crystal regions, with said grain boundary therebetween, wherein a first lattice image corresponding to the first crystal region has a first direction different from a second direction of a second lattice image corresponding to the second crystal region (as recited in lines 7-11 of claim 1), it would have been obvious to include said limitation in view of *Gates et al*, who, in a patent on the formation of a polysilicon film on a substrate (title and col. 6, l. 13) using CVD with seeding (see abstract), hence analogous to the art of Iwasaki (see his title and Examples 1 and 2 as cited in the rejection), teach the polysilicon film 44 to have several, hence also first and second, crystal regions with grain boundary in between (see Figures 3A, 3B, 4 and col. 5, l. 55 – col. 6, l.13). It can be concluded from the teaching by Gates et al that the typical result of the CVD method to make a polysilicon film is one that meets said limitation. The claim would have been obvious because following a closely related process for improving a particular class of devices was part of the ordinary skill in the art, in view of the teaching of the technique for improvement in other situations such as those taught by Gates et al.

With regard to claim 42, the direction of movements of any of the (charge) carriers has inherently two components, a random component and a component in response to the local (mainly electric) field. While the direction of said random component by its very nature is not subject to control, the component in response to the local field is a result of the operation of the device, and hence is not a limitation of the device as such.

Therefore, the limitation on the direction of movement of a carrier in said channel formation region is a statement of intended use not serving to patently distinguish the claimed structure over that of the reference as long as the structure of the cited reference is capable of performing the intended use. See MPEP 2111-2115. See also MPEP 2114 that states:

"A claim that contains a "recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus" if the prior art apparatus teaches all of the structural limitations of the claim Ex parte Masham, 2 USPQd 1647.".

"Claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function. In re Danly, 263 F.2d 844, 847, 120 USPQ 528, 531."

"Apparatus claims cover what is device is, not what a device does" Hewlett-Packard versus Bausch & Lomb Inc., 15 USPQ2d 1525, 1528."

In the underlying case, direction of movement of at least one carrier, in particular during the ON state, in said channel formation region coincides with, i.e., is parallel to, the direction of extension of said grain boundary, i.e., the direction along which said

grain boundary is extended (see, for instance Figures 2B and 3F (grain boundary extended along 23, which has portions parallel to the channel between source and drain 26N (see Figure 3I, e.g.). Therefore, the device of the prior art is capable of performing the intended use.

With regard to claim 43: the semiconductor film by Iwasaki comprises silicon (see Figure 3J and discussion, especially col. 10, l. 51 and Example 2).

With regard to claim 47: the only limitation additional to those of claim 21 is "a thermal oxidation film provided between the semiconductor film and the gate electrode". First it is observed that "thermal oxidation film" does not patentably distinguish from "oxide film", because the difference is one of manufacture, not necessarily of structure. Applicant is reminded that the limitation in the present product claim is only of patentable weight in as much as the method steps distinguish the final structure, and to the extent not impacting final structure are taken to be product-by-process limitations and non-limiting. A product by process claim is directed to the product per se, no matter how they are actually made. See In re Fessman, 180 USPQ 324, 326 (CCPA 1974); In re Marosi et al, 218 USPQ 289, 292 (Fed. Cir. 1983), and In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make clear that it is the patentability of the final structure of the product "gleaned" from the process steps that must be determined in a "product-by-process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not. Second, Iwasaki teaches a

silicon oxide gate insulating film 10 (col. 10, l. 14-18), and hence the limitation is met.

Although Iwasaki does not explicitly teach the limitation that said semiconductor film comprises first and second crystal regions, with said grain boundary therebetween, wherein a first lattice image corresponding to the first crystal region has a first direction different from a second direction of a second lattice image corresponding to the second crystal region (as recited in lines 7-11 of claim 1), it would have been obvious to include said limitation in view of *Gates et al*, who, in a patent on the formation of a polycrystalline film on a substrate (title) using CVD (see abstract), hence analogous to the art of Iwasaki (see his title and Examples 1 and 2 as cited in the rejection), teach the polysilicon film 44 to have several, hence also first and second, crystal regions with grain boundary in between (see Figure 4 and col. 6, l. 4-13). It can be concluded from the teaching by Gates et al that the typical result of the CVD method to make a polysilicon film is one that meets said limitation. The claim would have been obvious because following a closely related process for improving a particular class of devices was part of the ordinary skill in the art, in view of the teaching of the technique for improvement in other situations such as those taught by Gates et al.

With regard to claim 51, the direction of movements of any of the (charge) carriers has inherently two components, a random component and a component in response to the local (mainly electric) field. While the direction of said random component by its very nature is not subject to control, the component in response to the

local field is a result of the operation of the device, and hence is not a limitation of the device as such.

Therefore, the limitation on the direction of movement of a carrier in said channel formation region is a statement of intended use not serving to patently distinguish the claimed structure over that of the reference as long as the structure of the cited reference is capable of performing the intended use. See MPEP 2111-2115. See also MPEP 2114 that states:

"A claim that contains a "recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus" if the prior art apparatus teaches all of the structural limitations of the claim Ex parte Masham, 2 USPQd 1647.".

"Claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function. In re Danly, 263 F.2d 844, 847, 120 USPQ 528, 531."

"Apparatus claims cover what is device is, not what a device does" Hewlett-Packard versus Bausch & Lomb Inc., 15 USPQ2d 1525, 1528."

In the underlying case, direction of movement of at least one carrier, in particular during the ON state, in said channel formation region coincides with, i.e., is parallel to, the direction of extension of said grain boundary, i.e., the direction along which said grain boundary is extended (see, for instance Figures 2B and 3F (grain boundary extended along 23, which has portions parallel to the channel between source and drain 26N (see Figure 3I, e.g.). Therefore, the device of the prior art is capable of performing the intended use.

With regard to claim 52: the semiconductor film by Iwasaki comprises silicon (see Figure 3J and discussion, especially col. 10, l. 51 and Example 2).

2. ***Claims 22 and 48*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki and Gates et al as applied to claim 21 and claim 47, respectively, and in further view of Erhart et al. (USPAT 5,572,211) (previously cited).

As detailed above, claim 21 and claim 47 are unpatentable over Iwasaki et al in view of Gates et al. Iwasaki nor Gates et al necessarily teach the further limitation defined by claims 22 and 48. Iwasaki does teach the inclusion of TFTs in active matrix LCD displays for computers (column 1, lines 7-20).

However, it would have been obvious to include said further limitation in view of Erhart et al, who teach the inclusion of *capacitors*, e.g., 56 and 58 (column 6, line 55 – column 6, line 15), in addition to thin film transistors e.g., 48 and 50 (column 6, lines 55-60) in an active matrix display (column 6, lines 16-55) in a *personal* computer (column 12, lines 45-49). *Motivation* to include the teaching by Erhart in the device by Iwasaki derives at least from the obvious advantage to apply the invention to improvements of existing technology, i.e., to active matrix LCD displays in personal computers wherein capacitors store charge corresponding to the desired shade for the pixel electrode to which said storage capacitor pertains (column 6, line 64 – column 7, line 4). N.B.: said capacitors imply *auxiliary* capacitance because they are not part of the TFT, i.e., not part of the MOS capacitor that is part of the TFT.

3. ***Claims 23, 25, 46, 49-50 and 55*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki and Gates et al as applied to claim 21, and further in view of den Boer (USPAT 5,539,219) (previously cited).

On claim 23 and 49: As detailed above, claims 21 and 47 are unpatentable over Iwasaki in view of Gates et al. Iwasaki nor Gates et al necessarily teach the further limitation as defined by claims 23 and 49, although Iwasaki does teach the computer (col. 1, l. 15-20) to further comprise an active matrix type liquid crystal display device (col. 1, l. 7-20). Iwasaki does not specifically recited pixel electrode and opposite electrode, with liquid crystal provided therebetween.

However, said limitation merely conforms to the conventional active matrix liquid crystal display technology, as witnessed for instance by den Boer et al., who teach an active matrix liquid crystal display device (column 1, lines 5-33) to comprise not only TFTs 21 (column 4, line 62 – column 5, line 8) but also pixel electrode 51 (column 5, lines 5-8 and column 8, lines 33-43), common electrode 59 (column 8, lines 37-39) opposite said pixel electrode and hence qualifying as "opposite" electrode (see Figure 5) with liquid crystal 57 between said pixel electrode and said opposite electrode. *Motivation* to include said limitation as taught by den Boer in the invention by Iwasaki at least derives from the economy to apply the invention to already existing and hence easily marketable technology.

With regard to claims 25 and 50, Iwasaki does not specifically teach the further limitation on channel length as recited. However, it would have been obvious to include the limitation in view of den Boer, who teaches a channel length of about 2 μm to 4 μm

(column 8, lines 8-19) so as to achieve a reduction in pixel flickering, image retention and an improvement in gray level uniformity (see abstract). Applicant is reminded A *prima facie* case of obviousness typically exists when the ranges of a claimed composition overlap the ranges disclosed in the prior art or when the ranges of a claimed composition do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. In re Peterson, 65 USPQ2d 1379 (CA FC 2003). In the underlying case, the range in the prior art (about 2 to 4 μm) actually overlaps the range as claimed (less than or equal 2 μm) while motivation immediately derives from the teaching by den Boer that the shortened channel length enables reduction in pixel flickering and image retention and an improvement in grey level uniformity.

With regard to claims 46 and 55: the pixel electrode by den Boer comprises ITO (col. 7, l. 51). Motivation derives at least from the good conductivity and transparency of ITO, both qualities being important for an electrode in the way of light.

4. ***Claims 44-45 and 53-54*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki and Gates et al as applied to claims 21 and 47, in view of Kobayashi (3,925,803) (previously cited).

As detailed above, claims 21 and 47 are unpatentable over Iwasaki in view of Gates et al. Iwasaki nor Gates et al necessarily teach the further limitations of either claim 44 or 45, nor claims 53 or 54. However, it would have been obvious to include said further limitations in view of Kobayashi, who, in a patent on a field effect transistor, - in particular: on the polycrystalline structure of the channel region therein, hence

analogous art (TFTs are field effect transistors as well), teach the source/channel/drain region to comprise, within the channel region, rod-shaped silicon crystals 3 (col. 2, l. 30), evidently flattened at the top (Figure 1 and discussion in col. 2). *Motivation* derives at least from the noted high trans-conductance (see "Summary of the Invention", col. 1).

5. ***Claims 56 and 60-61*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki (JP 08-288515 A) (as cited above, again with Iwasaki (USPAT 5,759,879) used for translation) in view of Inoue et al (6,153,893) (previously cited) and Gates et al (5,830,538).

On claim 56: Iwasaki teaches (whole document, especially title, abstract, "Field of the Invention", column 1, lines 7-20, and Examples 1-2, columns 7-12; Figures 2-3) a semiconductor film 22 (column 10, lines 45-48) over a substrate 16 (loc.cit.) and comprising a source region and drain region (both 26N; see column 10, line 50) and a channel formation region 26i (column 10, lines 49-50) provided between said source and drain regions; and a gate electrode 25 (column 10, line 55) provided adjacent to said channel formation region with a gate insulating film 24 (column 10, line 54) therebetween; wherein lattices are continuously connected to each other at a grain boundary 23 (Figure 3F and column 12, lines 17-18) of said semiconductor film, inherently so, because a grain boundary is a boundary, i.e., a line, point or plane that indicates or fixes a limit or extent, between two grains, i.e., crystal grains; said crystal grains inherently having spatial extent, as otherwise their defining property, i.e., spatial periodicity, could not possibly exist; the lines denoting the grain boundaries in Figure 3F thus denote the limits on either side of the crystal grains connected by their common

grain boundaries, implying continuity across said grain boundaries; hence the lattices of said grains, extending by definition of the grains over their entire spatial domain, are continuously connected to each other at the grain boundaries of said semiconductor film.

Iwasaki does not necessarily teach the limitation of *"a low concentration impurity region provided between the channel formation region and at least one of the source region and the drain region".*

However, it would have been obvious to include said limitation in view of Inoue et al, who, in a patent on a thin film transistor (title, abstract), hence analogous art, teach the manufacture of a lightly doped drain (LDD) structure, known to be beneficial for insulated gate field effect transistors generally, for the specific advantage of prevention of pixel leakage (col. 2, l. 23-28), from which teaching *motivation* immediately follows.

With regard to claim 60: the direction of movements of any of the (charge) carriers has inherently two components, a random component and a component in response to the local (mainly electric) field. While the direction of said random component by its very nature is not subject to control, the component in response to the local field is a result of the operation of the device, and hence is not a limitation of the device as such.

Therefore, the limitation on the direction of movement of a carrier in said channel formation region is a statement of intended use not serving to patently distinguish the claimed structure over that of the reference as long as the structure of the cited

reference is capable of performing the intended use. See MPEP 2111-2115. See also MPEP 2114 that states:

"A claim that contains a "recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus" if the prior art apparatus teaches all of the structural limitations of the claim Ex parte Masham, 2 USPQd 1647.".

"Claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function. In re Danly, 263 F.2d 844, 847, 120 USPQ 528, 531."

"Apparatus claims cover what is device is, not what a device does" Hewlett-Packard versus Bausch & Lomb Inc., 15 USPQ2d 1525, 1528."

In the underlying case, direction of movement of at least one carrier, in particular during the ON state, in said channel formation region coincides with, i.e., is parallel to, the direction of extension of said grain boundary, i.e., the direction along which said grain boundary is extended (see, for instance Figures 2B and 3F (grain boundary extended along 23, which has portions parallel to the channel between source and drain 26N (see Figure 3I, e.g.). Therefore, the device of the prior art is capable of performing the intended use.

With regard to claim 61: the semiconductor film by Iwasaki comprises silicon (see Figure 3J and discussion, especially col. 10, l. 51 and Example 2).

6. ***Claim 57*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki, Inoue et al and Gates et al as applied to claim 56, in view of Erhart et al. (USPAT 5,572,211) (previously cited).

As detailed above, claim 56 is unpatentable over Iwasaki in view of Inoue et al and Gates et al. Neither Iwasaki nor Inoue et al nor Gates et al necessarily teach the further limitation defined by claim 57, although Iwasaki does teach the inclusion of TFTs in active matrix LCD displays for computers (column 1, lines 7-20).

However, it would have been obvious to include said further limitation in view of Erhart et al, who teach the inclusion of *capacitors*, e.g., 56 and 58 (column 6, line 55 – column 6, line 15), in addition to thin film transistors e.g., 48 and 50 (column 6, lines 55-60) in an active matrix display (column 6, lines 16-55) in a *personal* computer (column 12, lines 45-49). *Motivation* to include the teaching by Erhart in the device by Iwasaki derives at least from the obvious advantage to apply the invention to improvements of existing technology, i.e., to active matrix LCD displays in personal computers wherein capacitors store charge corresponding to the desired shade for the pixel electrode to which said storage capacitor pertains (column 6, line 64 – column 7, line 4). N.B.: said capacitors imply *auxiliary* capacitance because they are not part of the TFT, i.e., not part of the MOS capacitor that is part of the TFT.

7. ***Claims 58-59 and 64*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki, Inoue et al and Gates et al as applied to claim 56, in view of den Boer (USPAT 5,539,219) (previously cited).

As detailed above, claim 56 is unpatentable over Iwasaki in view of Inoue et al and Gates et al. Neither Iwasaki nor Inoue et al nor Gates et al necessarily teach the further limitation as defined by claim 58, although Iwasaki does teach the computer (col. 1, l. 15-20) to further comprise an active matrix type liquid crystal display device (col. 1, l. 7-20). Iwasaki does not specifically recited pixel electrode and opposite electrode, with liquid crystal provided therebetween.

However, said limitation merely conforms to the conventional active matrix liquid crystal display technology, as witnessed for instance by den Boer et al., who teach an active matrix liquid crystal display device (column 1, lines 5-33) to comprise not only TFTs 21 (column 4, line 62 – column 5, line 8) but also pixel electrode 51 (column 5, lines 5-8 and column 8, lines 33-43), common electrode 59 (column 8, lines 37-39) opposite said pixel electrode and hence qualifying as "opposite" electrode (see Figure 5) with liquid crystal 57 between said pixel electrode and said opposite electrode. *Motivation* to include said limitation as taught by den Boer in the invention by Iwasaki at least derives from the economy to apply the invention to already existing and hence easily marketable technology.

With regard to claims 59, Iwasaki does not specifically teach the further limitation on channel length as recited. However, it would have been obvious to include the limitation in view of den Boer, who teaches a channel length of about 2 μm to 4 μm (column 8, lines 8-19) so as to achieve a reduction in pixel flickering, image retention and an improvement in gray level uniformity (see abstract). Applicant is reminded A *prima facie* case of obviousness typically exists when the ranges of a claimed composition overlap

the ranges disclosed in the prior art or when the ranges of a claimed composition do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. In re Peterson, 65 USPQ2d 1379 (CA FC 2003). In the underlying case, the range in the prior art (about 2 to 4 μm) actually overlaps the range as claimed (less than or equal 2 μm) while motivation immediately derives from the teaching by den Boer that the shortened channel length enables reduction in pixel flickering and image retention and an improvement in grey level uniformity.

With regard to claim 64: the pixel electrode by den Boer comprises ITO (col. 7, l. 51). Motivation derives at least from the good conductivity and transparency of ITO, both qualities being important for an electrode in the way of light.

8. ***Claims 62-63*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki, Inoue et al and Gates et al as applied to claim 56, in view of Kobayashi (3,925,803).

As detailed above, claim 56 is unpatentable over Iwasaki in view of Inoue et al and Gates et al. Neither Iwasaki nor Inoue et al nor Gates et al necessarily teach the further limitation of claims 62 or 63. However, it would have been obvious to include said further limitations in view of Kobayashi, who, in a patent on a field effect transistor, - in particular: on the polycrystalline structure of the channel region therein, hence analogous art (TFTs are field effect transistors as well), teach the source/channel/drain region to comprise, within the channel region, rod-shaped silicon crystals 3 (col. 2, l. 30), evidently flattened at the top (Figure 1 and discussion in col. 2). *Motivation* derives at least from the noted high trans-conductance (see "Summary of the Invention", col. 1).

9. ***Claim 65*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki and Gates et al as applied to claim 21 above, and further in view of Okada (5,582,640) (cited previously in the Office Action mailed 4/19/05).

As detailed above, claim 21 is unpatentable over Iwasaki in view of Gates et al. Neither Iwasaki nor Gates et al necessarily teach the further limitation defined by claim 65.

However, it would have been obvious to include said further limitation in view of Okada et al, who, in a patent on the manufacture of a single crystal or high quality polycrystalline silicon crystal (e.g., 27th Embodiment, columns 63-64, and abstract and title), hence art analogous to Iwasaki, *diagnosed the channel formation region inter alia by the use of TEM (col. 64, l. 9) and found that any grain boundaries pertain to very large size grains (of the order of 1200 A; col. 64); furthermore, Okada et al state that said grain boundaries do not substantially impede the mobility of charge carriers in the thin film transistor (col. 64, l. 40-45).* It would furthermore have been obvious to make the semiconductor thin film without crystal defects observable by TEM according to the third embodiment (col. 33, l. 62 – col. 23). *Motivation* to include the teaching of the third embodiment by Okada et al thus derives from the absence of a deterioration in electron mobility due to crystal defects.

10. ***Claim 66*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki and Gates et al as applied to claim 47 above, and further in view of Okada (5,582,640) (cited previously in the Office Action mailed 4/19/05).

As detailed above, claim 47 is unpatentable over Iwasaki in view of Gates et al. Neither Iwasaki nor Gates et al necessarily teach the further limitation defined by claim 66.

However, it would have been obvious to include said further limitation in view of Okada et al, who, in a patent on the manufacture of a single crystal or high quality polycrystalline silicon crystal (e.g., 27th Embodiment, columns 63-64, and abstract and title), hence art analogous to Iwasaki, *diagnosed the channel formation region inter alia by the use of TEM (col. 64, l. 9) and found that any grain boundaries pertain to very large size grains (of the order of 1200 A; col. 64); furthermore, Okada et al state that said grain boundaries do not substantially impede the mobility of charge carriers in the thin film transistor (col. 64, l. 40-45).* It would furthermore have been obvious to make the semiconductor thin film without crystal defects observable by TEM according to the third embodiment (col. 33, l. 62 – col. 23). *Motivation* to include the teaching of the third embodiment by Okada et al thus derives from the absence of a deterioration in electron mobility due to crystal defects.

11. ***Claim 67*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki and Gates et al as applied to claim 56 above, and further in view of Okada (5,582,640) (cited previously in the Office Action mailed 4/19/05).

As detailed above, claim 56 is unpatentable over Iwasaki in view of Gates et al. Neither Iwasaki nor Gates et al necessarily teach the further limitation defined by claim 67.

However, it would have been obvious to include said further limitation in view of Okada et al, who, in a patent on the manufacture of a single crystal or high quality polycrystalline silicon crystal (e.g., 27th Embodiment, columns 63-64, and abstract and

title), hence art analogous to Iwasaki, *diagnosed the channel formation region inter alia by the use of TEM (col. 64, l. 9) and found that any grain boundaries pertain to very large size grains (of the order of 1200 A; col. 64); furthermore, Okada et al state that said grain boundaries do not substantially impede the mobility of charge carriers in the thin film transistor (col. 64, l. 40-45).* It would furthermore have been obvious to make the semiconductor thin film without crystal defects observable by TEM according to the third embodiment (col. 33, l. 62 – col. 23). *Motivation* to include the teaching of the third embodiment by Okada et al thus derives from the absence of a deterioration in electron mobility due to crystal defects.

12. ***Claim 68*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki and Gates et al as applied to claim 21 above, and further in view of Tran et al (5,534,445).

As detailed above, claim 21 is unpatentable over Iwasaki in view of Gates et al. Neither Iwasaki nor Gates et al necessarily teach the further limitation defined by claim 68.

However, it would have been obvious to include said further limitation in view of Tran et al, who, in a patent on polysilicon-based thin film transistors, teach to select a silicon wafer for providing a substrate underneath the insulating layer on which the semiconductor film is grown (Figure 1 and col. 4, l. 3-7). *Motivation* to include the teaching by Tran et al derives from the suitability of silicon wafers in the art of integrated circuitry in which the thin film transistors are often used and which is shown by Tran et

al to be compatible with very low current leakage (abstract and "Detailed Description of the Invention").

13. ***Claim 69*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki and Gates et al as applied to claim 21 above, and further in view of Tran et al (5,534,445).

As detailed above, claim 47 is unpatentable over Iwasaki in view of Gates et al. Neither Iwasaki nor Gates et al necessarily teach the further limitation defined by claim 68.

However, it would have been obvious to include said further limitation in view of Tran et al, who, in a patent on polysilicon-based thin film transistors, teach to select a silicon wafer for providing a substrate underneath the insulating layer on which the semiconductor film is grown (Figure 1 and col. 4, l. 3-7). *Motivation* to include the teaching by Tran et al derives from the suitability of silicon wafers in the art of integrated circuitry in which the thin film transistors are often used and which is shown by Tran et al to be compatible with very low current leakage (abstract and "Detailed Description of the Invention").

14. ***Claim 70*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki and Gates et al as applied to claim 21 above, and further in view of Tran et al (5,534,445).

As detailed above, claim 56 is unpatentable over Iwasaki in view of Gates et al. Neither Iwasaki nor Gates et al necessarily teach the further limitation defined by claim 68.

However, it would have been obvious to include said further limitation in view of Tran et al, who, in a patent on polysilicon-based thin film transistors, teach to select a silicon wafer for providing a substrate underneath the insulating layer on which the semiconductor film is grown (Figure 1 and col. 4, l. 3-7). *Motivation* to include the teaching by Tran et al derives from the suitability of silicon wafers in the art of integrated circuitry in which the thin film transistors are often used and which is shown by Tran et al to be compatible with very low current leakage (abstract and "Detailed Description of the Invention").

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

15. ***Claims 21, 44 and 45*** are rejected on the ground of non-statutory obviousness double patenting as being unpatentable over claim 5 of US Patent 6,380,560 B1 in view of Gates et al (5,830,538).

An obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but an examined application claim is not patentably distinct from the reference claims because the examined claim is either anticipated by, or would be obvious over, the reference claims. See, e.g., In re Berg 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985). Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 21 is generic to all that is recited in claim 5 of US Patent 6,380,560, except for the additional limitations on first and second crystal regions and corresponding first and second lattice images as recited in independent claims 21, 47 and 56. In other words, claim 5 of US Patent 6,380,560 fully encompasses the subject matter of claim 1 of the current application, except for said additional limitations.

Specifically, within the Markush claim 5 the selection "personal computer" for the claimed semiconductor device renders claim 21 fully encompassed by the limitations of its independent claim 1, because of the following mapping:

- Semiconductor film in claim 21: semiconductor film in claim 5 through claim 1.

- Substrate in claim 21: anticipated by "single crystal semiconductor wafer" in claim 5 through claim 1, said single crystal semiconductor wafer being a special kind of substrate.
- Source region, drain region and channel formation region of claim 21: idem claim 5 through claim 1.
- Gate electrode adjacent said channel formation region with a gate insulating film therebetween in claim 21: idem claim 5 through claim 1.
- The limitation "wherein lattice are continuously connected to each other at a grain boundary of said semiconductor film" in claim 21: is anticipated through the limitation "wherein lattices are continuously connected to each other at substantially all of said grain boundary according to high resolution TEM", with said "grain boundary being defined by "adjacent two crystals"
- With regard to claims 44 and 45, their limitations are also anticipated by those of claims 6 and 7 of 6,380,560, because said two crystals having said grain boundary are comprised in the semiconductor film.

Although, as mentioned, said patent does not recite aforementioned additional limitations in the claimed invention, it would have been obvious to include said additional limitations in view of Gates et al, who, in a patent on the formation of a polysilicon film on a substrate (title and col. 6, l. 13) using CVD with seeding (see abstract), hence analogous to the art of Iwasaki (see his title and Examples 1 and 2 as cited in the rejection), teach the polysilicon film 44 to have several, hence also first and

second, crystal regions with grain boundary in between (see Figures 3A, 3B, 4 and col. 5, l. 55 – col. 6, l.13). It can be concluded from the teaching by Gates et al that the typical result of the CVD method to make a polysilicon film is one that meets said limitation. The claim would have been obvious because following a closely related process for improving a particular class of devices was part of the ordinary skill in the art, in view of the teaching of the technique for improvement in other situations such as those taught by Gates et al. Finally, there is no reason why aforementioned additional limitations could not have been claimed in said patent 6,380,560, as witnessed by Figures 17 and their discussion.

Response to Arguments

Applicant's arguments filed 8/20/07 have been fully considered but they are not persuasive. First argument in traverse of rejections of claims 21, 42, 47, 51 and 52 in Remarks (page 8 of Amendment) do not persuade at least in view of Gates et al: see rejections overhead, herewith incorporated by reference in their entirety in response to Applicant's argument. Applicant's argument in traverse of the rejection of claims 56, 60 and 61 and in traverse of the rejection of claims 22 and 48, as well as applicant's argument in traverse of the rejection of claim 23, 25, 46, 50 and 55 and of claims 44, 45, 53 and 54 all rely exclusively on said first argument and are refuted by the rejections of said claims as presented overleaf, which are herewith included by reference in their entirety. With regard to the double patenting rejection, counter to applicant's argument in traverse thereof, an obviousness double patenting rejection is in order, because the newly added limitations are at least obvious over Gates et al, with reference to the

double patenting rejection overleaf, said double patenting rejection herewith being included by reference in its entirety in this response.

The newly added claims have been examined for the first time in this particular context, and are found to be unpatentable: see the rejections of claims 65-70. Examiner notes, however, that the issue on claim language including the high resolution TEM (claims 65-67) has been extensively commented upon in the Office Action mailed 4/19/2005.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Bourret, Alain, "Grain Boundaries in Semiconductors", Chapter 7 in "Handbook of Semiconductor Technology", John Wiley & Sons, New York (2002), Volume 1, pp. 382-404, especially, section 7.1, first sentence. Not prior art, but presented as evidence that the claim language as amended, almost always is satisfied.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JPM

October 25, 2007

Primary Patent Examiner:

Johannes Mondt (TC3600, Art Unit: 3663)